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# Hybrid PV HgCdTe Detectors: Technology Reliability and Failure Physics Program

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# SECTION 1
# INTRODUCTION

## 1.1 PROGRAM GOALS

$Hg_{1-x}Cd_xTe$ focal planes are finding greater application in systems designed to operate in the medium wave (MW) and long wave (LW) infrared bands. Prior to those focal planes being deployed in the field, it is important to understand the potential failure mechanisms to permit high reliability units to be built. Indium bump bonding (also known as flip-chip bonding or hybridization) is a widespread method for providing electrical interconnect and mechanical support of these focal planes to circuit boards or silicon (Si) multiplexers. This program was designed to evaluate the effect of the hybridization process on MW focal planes, as well as to assess their long term stability.

## 1.2 TECHNICAL APPROACH

To address hybridization and reliability issues, Honeywell undertook a two step approach. The studies included:

### 1.2.1 Hybridization Force Study

This was an evaluation of the effect of forces used during hybridization on defect levels in the HgCdTe liquid phase epitaxy (LPE) layer and the CdTe substrate. The correlation of device performance with measured defect level was also examined.

### 1.2.2 Environmental Stress Testing

This task examined three conditions which can potentially affect the performance of hybridized detector arrays.

- LONG TERM STORAGE - This task evaluated the stability of MW HgCdTe detector arrays after two years storage at room temperature in dry nitrogen.
- VACUUM BAKE - To maintain vacuum integrity, dewars are baked during the pumping cycle. In addition, ambient storage temperatures can occasionally be high. The effect of high temperature (85 °C) on the performance hybridized detector arrays was evaluated.
- TEMPERATURE CYCLING - HgCdTe detector arrays are often hybridized directly to Si muxes. As a result of the mismatch in thermal expansion coefficients between HgCdTe and Si, significant lateral motion can occur during cooldown from temperature to operating temperature (typically 80 K). This can cause strain in the In column interconnects, especially for large focal plane arrays. The resultant strain can also be transformed to the detector array, and could potentially affect device performance. This task investigated the effect of temperature cycling on interconnect yield and device performance.

# SECTION 2
# EXPERIMENTS/RESULTS

## 2.1 MATERIAL GROWTH AND DETECTOR ARRAY FABRICATION

In support of the technical tasks, six single layer, MW LPE films were grown with 80 K cutoff wavelength ranging from 4.1 to 4.7 $\mu$m (Table 2-1).

The films were intentionally grown to shorter wavelength to increase the detector $R_o$. Arrays were fabricated in a 240 x 8 element configuration, approximately 380 mil in length. This was designed to maximize the effect of thermal expansion coefficient mismatch between the $Hg_{1-x}Cd_xTe$ array and Si multiplexer to which the arrays were hybridized. The detector arrays were fabricated with 25 $\mu$m tall indium columns. This was designed to maximize the ability of the indium to flow during hybridization, resulting in better cold welding and reduction of stress on the $Hg_{1-x}Cd_xTe$. Unfortunately, the spectral response of the detectors was attenuated at wavelengths below the cutoff wavelength and the arrays exhibited low overall quantum efficiency as a result. They were therefore not used for deliveries. Instead, arrays fabricated earlier on another program were employed. These arrays were in a 32 x 32 mil configuration with a 4 mil pitch (Figure 2-1). In addition, LW detector arrays (test arrays from the 240 x 8 mask set) from the MDAC 240 FPA Program were also used for temperature cycling studies.

**Table 2-1. LPE Film Summary for NRL Program**

| FILM ID | DATE | $\lambda$ CUTOFF ($\mu$m) | THICKNESS ($\mu$m) | CARRIER CONCENTRATION ($cm^{-3}$) | MORPHOLOGY | STREAKS | SCRATCHES |
|---|---|---|---|---|---|---|---|
| MW299 | 1 22 87 | 4.33 | 20 | $9.0x10^{15}$ | Excellent | None | No |
| MW300 | 1 26 87 | 4.25 | 18 | ($9.0x10^{15}$) | Excellent | None | One |
| MW301 | 1 27 87 | 4.25 | 18 | $4.0 \times 10^{15}$ | Excellent | None | No |
| MW302 | 1 28 87 | 4.1 | 16 | $9.0x10^{15}$ | Excellent | None | No |
| MW303 | 1 29 87 | 3.95 | 22 | $8.0x10^{15}$ | Excellent | None | No |
| MW304 | 1 30 87 | 3.95 | 20 | $7.0x10^{15}$ | Excellent | None | No |

## 2.2 HYBRIDIZATION FORCE STUDY (HFS)

*The following discussion of the HFS is in large part a reprint of the paper "Etch Pit Study of Dislocation Formation in $Hg_{1-x}Cd_xTe$ During Array Hybridization and Its Effect on Device Performance" by Peter W. Norton and Anthony P. Erwin, presented at the 1988 Workshop on the Physics and Chemistry of Mercury Cadmium Telluride.*

The relationship between hybridization force, dislocation (etch pit) density and device performance has been investigated for devices fabricated from $Hg_{1-x}Cd_xTe$ LPE material. Cold-welded indium column interconnects are the predominant method used to mechanically and electrically attach mosaic arrays to silicon multiplexers. The mismatch in thermal expansion between the $Hg_{1-x}Cd_xTe$ photodiode arrays and silicon multiplexers stresses the interconnects when the arrays are cooled to their operating temperature (typically 40 K to 120 K) which can lead to failures. Increased hybridization force improves the mechanical stability of the interconnects but can introduce dislocations in the $Hg_{1-x}Cd_xTe$. Dislocations have been reported to degrade the performance of some device structures[3,4]. The dislocation density in the LPE film after growth was $\approx 8 \times 10^5/cm^2$. We have found no significant change in dislocation density at hybridization forces up to $\approx 3.9 \times 10^7$ N/m$^2$. At forces on the order of $5.9 \times 10^7$ N/m$^2$ ($\approx$ 10% of the Vickers Hardness[1]), the dislocation density in the films increased to $90 \times 10^5/cm^2$ in the areas where the indium columns were. The diffusion limited performance of the test structures at 120 K was not significantly degraded by the increased dislocation density. At 80 K however, where the devices were modeled to be g-r limited, there was an increase in dark current with increased dislocation density. The structures used in the study were fabricated from LPE $Hg_{1-x}Cd_xTe$ grown on a CdTe substrate. Implantation of boron into the p-type material through a ZnS passivation layer was used to form junctions. A zero bias junction resistance of 1000 to 7000 $\Omega$-cm$^2$ was typical for the test structures which had a cutoff wavelength of 4.7 $\mu$m at 120 K.

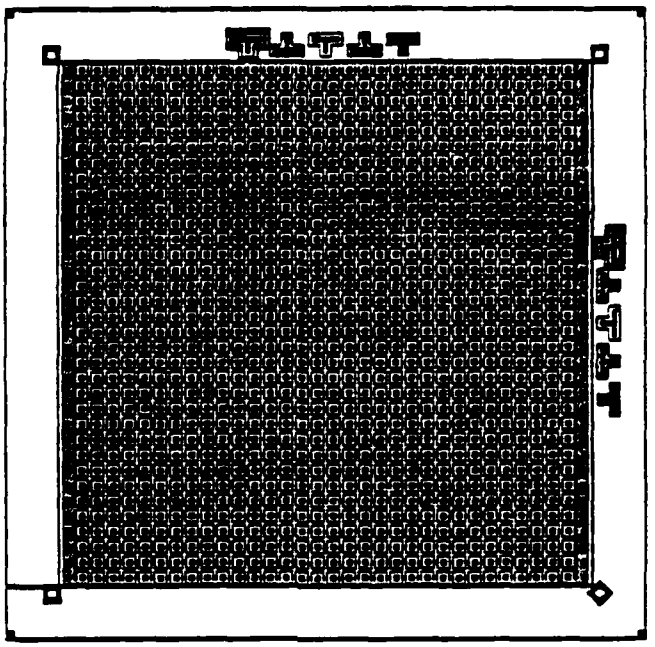
### 2.2.1 Introduction

Hybrid mosaic HgCdTe focal plane arrays have become an important part of advanced infrared detector technology. The most commonly used approach for attaching mosaic HgCdTe photodiode arrays to their silicon readout multiplexers, both mechanically and electrically, is the use of indium column interconnects[2]. Indium columns, fabricated onto both the HgCdTe array and Si multiplexer, are coldwelded together during hybridization processes which often involve heat and force. In general, using increased force during the hybridization process results in improved interconnect reliability, but can also introduce dislocations in the epitaxial HgCdTe crystal. Miyamoto et. al.[3] and Tregilgas et. al.[4] have reported that the performance of MIS device structures at 77 K in $Hg_{0.8}Cd_{0.2}Te$ are sensitive to dislocation density. The purpose of this study was to determine the extent to which dislocation (as determined by etch pitting) are introduced during the hybridization process and their effect on $Hg_{0.7}Cd_{0.3}Te$ photodiode electrical characteristics.

### 2.2.2 Experimental Procedure

The procedure for this study was as follows. Fabricated 32 x 32 element photodiode arrays were hybridized to alumina leadout boards with a range of hybridization forces. The photodiode arrays were then electrically and radiometrically characterized for zero bias impedance, responsivity, and spectral response at several temperatures. After electrical characterization was

DETECTOR ARRAY LAYOUT



CIRCUIT BOARD LAYOUT

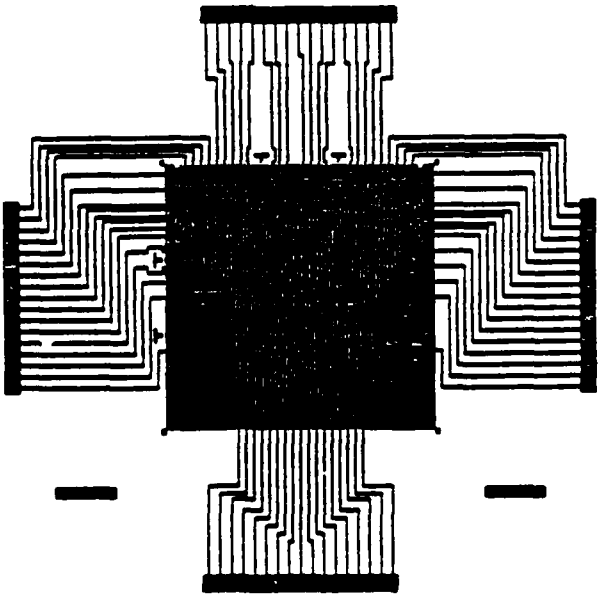


**Figure 2-1. Array Configuration Used to Investigate Hybridization Stress**

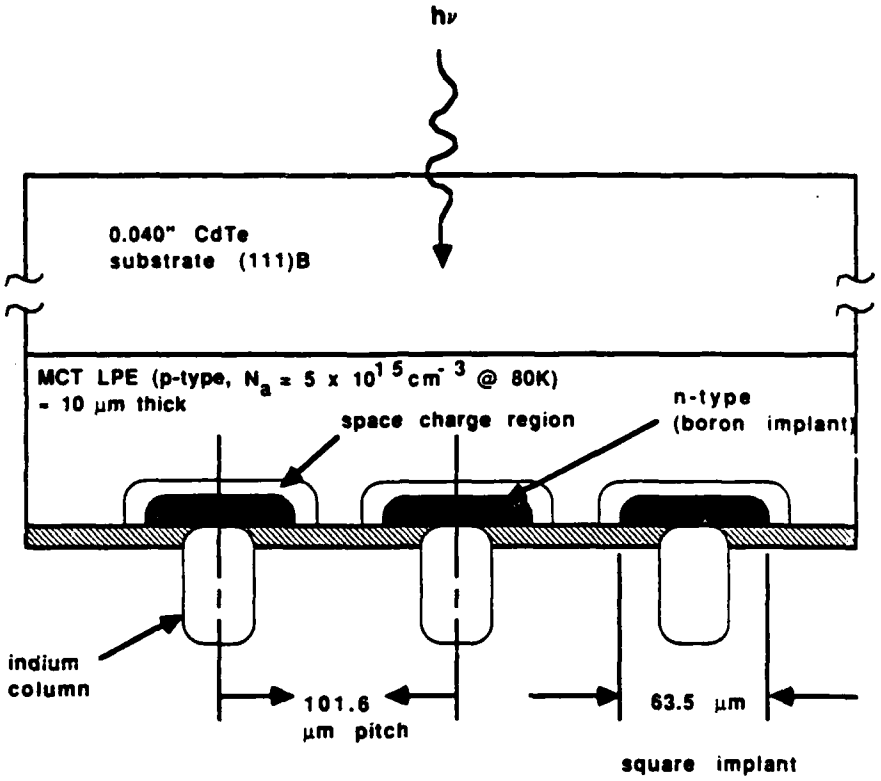



**Figure 2-2. Cross-section of Part of Photodiode Array.** Note the Location of the Implanted Junction with Respect to the Indium Column Interconnects

completed, the arrays were analyzed for etch pit density. In addition, two arrays which had not been hybridized were analyzed for etch pit density as control samples.

### 2.2.2.1 Description of Photodiode Arrays Used in the Study

All the photodiode arrays used in the study were fabricated from a single $Hg_{0.694}Cd_{0.306}Te$ wafer grown at Honeywell EOD in 1985. The 15 μm thick LPE layer was grown on the (111)B face of a 0.040" thick CdTe substrate using a horizontal slider system and Te-rich solution[5] at a growth temperature of 500 °C. The layer was annealed in a Hg overpressure to be p-type (Hg vacancy), had a carrier concentration of about 5 x $10^{15}$ $cm^{-3}$ and hole mobility of 275 $cm^2V^{-1}s^{-1}$ at 80 K as determined by Hall measurements. The planar $n^+$-on-p photodiode junctions were formed by boron ion implantation (200 keV, dosage = 1 x $10^{13}$ $cm^{-2}$) through a 0.5 μm thick ZnS passivation layer. There was no post implant anneal. The implanted area of each photodiode was 63.5 μm square on a 101.6 μm x and y pitch. The 32 x 32 element mosaic arrays had common p-side contact metallization along two sides. The 1156 evaporated indium interconnects were 30 μm square (as fabricated) and located directly on the implanted junctions, as the cross sectional view in Figure 2-2 illustrates. The CdTe substrates through which the radiation was incident was AR coated with 0.5 μm of ZnS. The arrays were fabricated in January, 1986 and stored in a dry nitrogen atmosphere until their use.

The arrays were hybridized to leadout boards fabricated from metallized alumina substrates, which gave electrical access to 64 individual photodiodes uniformly distributed about the array. The remaining elements are shorted to ground. Arrays were hybridized with forces from 1.4 to 9.4 x $10^7$ $N/m^2$. The hybridization system was a modified Research Devices Model M9 bump bonder. The M9 utilizes an autocollimator to establish planarity between the array and leadout

**Table 2-2. Summary of the Average Array Performance Data at 120 K for Four Arrays.** Array RH21-D3 and RH21-C3 showed increased EPD across the array which suggests that the hybridization force was not uniformly distributed across the array

| Array # | Hybridization Force (x 107 N/m2) | $R_oA$ (120K) ($\Omega cm^2$) | Q.E. (%) | Cutoff (120K) ($\mu m$) | EPD HgCdTe (x $10^5/cm^2$) | EPD CdTe (x $10^5/cm^2$) |
|---|---|---|---|---|---|---|
| RH21-E2 | 1.4 | 1200 | >80 | 4.69 | 3-5 | 2.6-4.12 |
| RH21-B4 | 4.1 | 5900 | >80 | 4.67 | 2-7 | 4.4-5.0 |
| RH21-D3 | 4.8 | 2500 | >80 | 4.66 | 4-7 and 21-56 | 14 |
| RH21-C3 | 9.4 | 4100 | >80 | 4.69 | 30-40 and 72 | 4.3-12 and >40 |

board to about 0.1 mr and monitors the hybridization force with an inline force indicator transducer to ±5% of the reading. The arrays were maintained at the hybridization force for ten minutes before being removed.

### 2.2.2.2 Hybridized Array Testing

The arrays were mounted in 68-pin flatpacks and tested in variable temperature liquid nitrogen dewars capable of attaining operating temperatures between 80 K and 300 K. Complete testing of array performance was done at T = 120 K, 150 K and 180 K. Junction impedance at zero bias (Ro), signal, and current versus voltage (I-V) measurements were taken with a 9° field-of-view coldshield. A bandpass filter with a 4.2 $\mu$m center wavelength and 0.26 $\mu$m bandwidth was attached to the coldshield, allowing a background photon flux $Q_B$ of 3.6 x $10^{13}$ photons $cm^{-2}$ s to be incident on the CdTe surface during testing.

In addition, limited characterization data (Ro and I-V curves) were taken at T = 80 K. Because of low dark current levels at this temperature, a high-amplification, low-noise test setup was used to measure device Ro and I-V curves. A full cold shield ($Q_B$ = 3 x $10^{10}$ photon $cm^{-2}$ s) was used to attain low photocurrent levels to reduce the photocurrent shot noise and to gain the most sensitivity from the amplifier. The photocurrent was also reduced to attain the most accurate zero bias impedance measurements from the near zero bias current-voltage slope which will change when a large photocurrent is present. The dewar was enclosed in a shielded box to minimize noise pickup.

The relative spectral response and relative quantum efficiency of the devices were measured without a coldshield at T = 120 K using a Nicolet Model 7199 Fourier Transform Spectrometer. The test data shown in Table 2-2 displays uniform array cutoff wavelength and quantum efficiencies greater than 80% on average for the four arrays studied.

### 2.2.2.3 Etch Pit Formation

After electrical characterization, the arrays were evaluated for etch pit density. The dislocation etches used in the study were the Nakagawa[6] or "N" etch for the CdTe, and a modified Polisar No. 2 etchant[7] or "P" etch for the HgCdTe. Both dislocation etches work on the (111)A face of the materials.

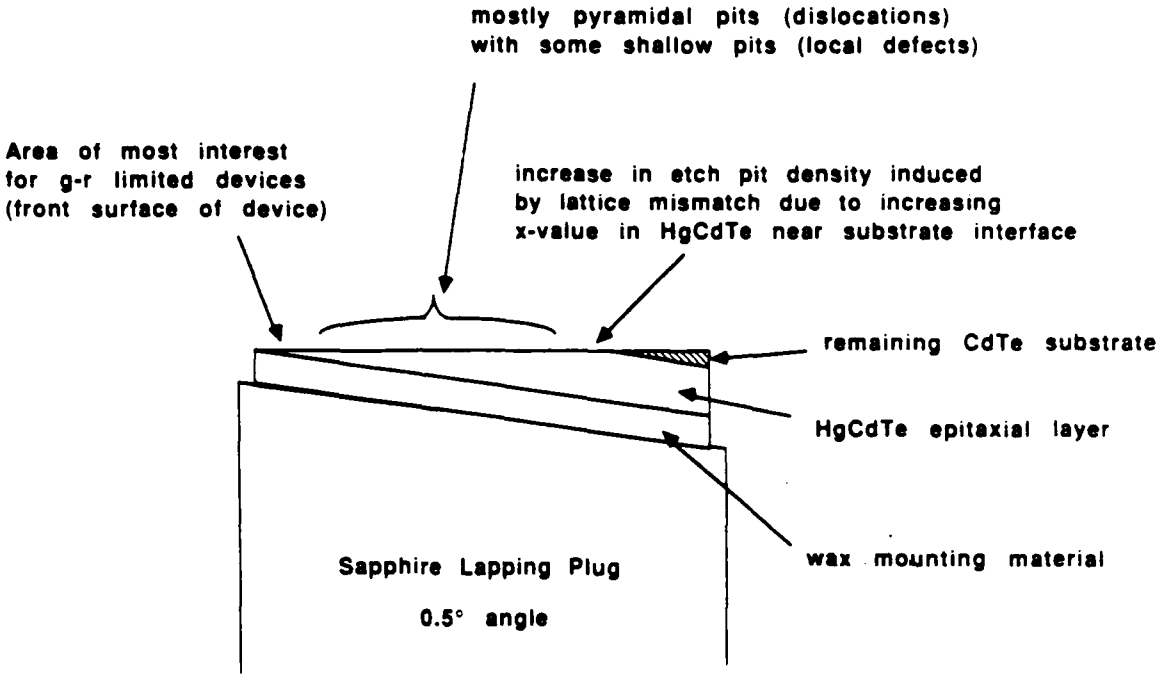



**Figure 2-3. Sample Mounted to Sapphire Angle Lapping Plug**

The composition of the P etch was: 180 ml $H_2O$, 60 ml $HNO_3$, 25 ml HCl, 5 ml $CH_3COOH$ and 0.1 ml Br. Best results were obtained when the solution aged at room temperature for 30 minutes and was then heated to 45 °C. The samples were held face down and steady in the etch solution for 30 to 60 seconds depending upon how soon bubbles became visible on the HgCdTe surface.

The arrays were carefully removed from their leadout boards by dissolving the indium interconnects in a hydrochloric acid solution. The arrays were then mounted with paraplast to a sapphire angle (0.5 °) lapping plug, epitaxial HgCdTe layer down ((111)A side up). The substrates were lapped with a 2% bromine in methanol solution to within about 100 $\mu$m of the interface. The N etch was then used to determine the etch pit density in the CdTe substrate. Further lapping of the samples with the 2% bromine in methanol solution exposed a cross section of the HgCdTe epitaxial layer, and surface reflectance measurements were taken to determine the x-value profile.[8] Etch pits were then formed ir the HgCdTe epitaxial layer with the P etch with an emphasis on obtaining accurate etch pit density measurements in the bulk and near the frontside of the layers where the space charge region of the photodiodes is located. Figure 2-3 illustrates the orientation of the samples and distribution of the etch pits. The lapping/etch pitting was repeated one to two times to establish the areal dependence of the etch pit density across the arrays.

The pits were etched large enough so that their structure could be examined under an optical microscope at moderate magnification levels (480X). Pits that were pyramidal in shape and came to a point as illustrated in Figure 2-4 were counted while pits that did not come to a point were attributed to the etch or localized defects and were not counted[9].

The large size of the pits limited the areas in which the etch pit density (EPD) could be accurately determined. In the graded x-value region approaching the epilayer/substrate inter-

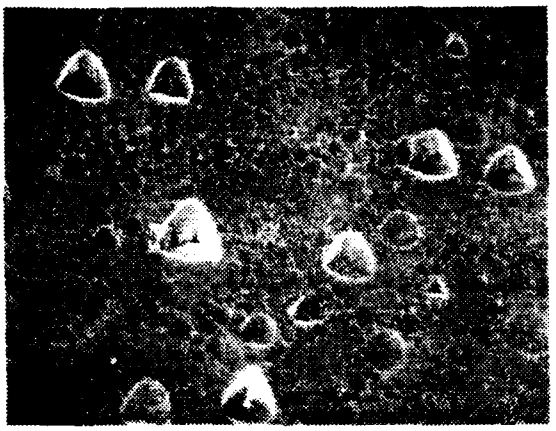


**Figure 2-4. Photomicrograph of Etch Pits on the (111) A Face of the HgCdTe LPE Layer.** The etch pits were obtained with the modified Polisar No. 2 etchant. Etch pits are about 3 microns across and have a depth of about 1 micron.

face, the EPD increases to the point where the overlap of the pits makes their density determination difficult. Variations in EPD at the HgCdTe/CdTe interface were not measured in this study.

The depth of the pits, on the order of 1 $\mu$m, limits the accuracy of the etch pit density measurements at the surface of the films. Near the surface, the etch pits extend completely through the film and therefore one cannot distinguish between pits that come to a point and those that are rounded. The effect of this on our measurements is discussed further in Section 2.2.4. We therefore used the etch pit density measured at approximately 1.5 to 2 $\mu$m below the surface to correlate the measured electrical properties of photodiodes near the sampled areas.

### 2.2.3 Results and Discussion

#### 2.2.3.1 Results in the CdTe Substrate from the Nakagawa Etch

The four samples examined for EPD in the CdTe layer were hybridized with $1.4 \times 10^7$, $4.1 \times 10^7$, $4.8 \times 10^7$ and $9.4 \times 10^7$ N/m$^2$. It should be noted that the maximum force allowable (for a given x-value) before which dislocations are introduced in the lattice is a function of a number of parameters. These include the geometry of the indium column, the density of the indium (related to the column formation process) and the manner in which the force is applied. The geometry and density of the column affect the maximum force due to their influence on the manner in which the column can deform under load. Short, broad columns are less able to expand, and hence the load is transferred directly to the underlying lattice. Since indium will flow under relatively low force, it is important to keep the rate of force application as slow as practical, to permit good column compression and cold welding while minimizing the transfer of force to the underlying lattice. Honeywell's approach has been to fabricate columns with high aspect ratio (tall and relatively narrow) and apply the force in slow, stepped increments. This has resulted in the ability to achieve large hybridization

forces with minimal lattice damage. The three samples hybridized at the lower forces all had EPD in the 3-5 x $10^5/cm^2$ range which is typical of the CdTe substrates prior to the growth of the epitaxial HgCdTe layer. The sample hybridized with the largest force however (RH21-D3), did show a large increase in EPD over the other samples. The EPD in the CdTe substrate of RH21-D3 ranged from 1 x $10^6 cm^{-2}$ along one side of the array and increased linearly across the array to greater than 6 x $10^6$ $cm^{-2}$. From the low magnification photomicrograph in Figure 2-5, one can see the increase in EPD across the array which suggests that the hybridization force was distributed unevenly across the array. We therefore infer that the array was not parallel to the leadout board during hybridization. We also infer that damage was introduced into the CdTe at forces less than 9.4 x $10^7 N/m^2$ as the lowest EPD (1 x $10^6$ $cm^{-2}$) was twice that seen on the arrays hybridized at lower forces.

### 2.2.3.2 Results in the HgCdTe Epilayers

Typical pyramidal EPD versus depth profiles for the two control samples (which had not been hybridized and tested) and for arrays hybridized with up to 4 x $10^7$ $N/m^2$ appear in Figure 2-6. The average EPD for most of the area near the surfaces is 8-9 x $10^5/cm^2$. In most of the samples there was a slight increase in EPD (10-12 x $10^5/cm^2$) at the surface. We could not distinguish between pointed and rounded pits at the surface because the pits extended completely through the films; we therefore do not know if the increased EPD at the surface was real. The increase at the surface could be a result of our experimental method or if real, may be induced by stresses from the ZnS passivation layer. We believe our etch pit density measurements near the surface to be accurate within a factor of 2-3.

In arrays hybridized with forces greater than or equal to 4.8 x $10^7$ $N/m^2$, increased EPD was observed over all or parts of the arrays, as listed in Table 2-2.

Array RH21-C3, hybridized at 4.8 x $10^7$ $N/m^2$ was the array hybridized at the lowest force where the EPD varied from the control samples. In this sample, the EPD at the array surface, along one edge of the array, was determined to be 5.6 x $10^6/cm^2$ but quickly reduced to 2.1 x $10^6/cm^2$ only a few microns beneath the surface. The increased EPD appeared in the area of the ground contact and therefore was not caused by implantation damage. The EPD also decreased laterally from the edge so that most of the array had an EPD of 8-12 x $10^5/cm^2$. Because the EPD was not uniform across the array but increased on one side, the array was probably not parallel to the substrate during hybridization so the force in the area of increased EPD was greater than 4.3 x $10^7$ $N/m^2$. This is as close an estimate as we can make to the critical force at which extended damage can be introduced into the HgCdTe epitaxial (III) layer.

Array RH21-C2, hybridized at 5.8 x $10^7$ $N/m^2$, showed a spatial distribution of EPD having the same spatial periodicity as the indium columns. At the column locations, the EPD was 9.6 x $10^6/cm^2$ and between columns was 2.1 x $10^6/cm^2$. The low magnification photomicrograph in Figure 2-7, illustrates the variation in EPD in the array. The figure shows angle-lapped Array RH21-C2, in which the damage extends completely through the epilayer, which was about 10$\mu$m thick.

### 2.2.3.3 Correlation of EPD Data and Electrical Test Data

Maps were generated for each of four arrays which included 120 K and 80 K zero bias impedance data and also the average EPD for the area. Because we did not measure the EPD of each photodiode, there was some uncertainty in EPD value assigned to particular photodiodes, which we estimate to be as much as a factor of two.

A plot of $R_oA$ versus EPD for the four arrays is shown in Figure 2-8. There is a trend in both the 120 K and 80 K data that $R_oA$ degrades with increased EPD.

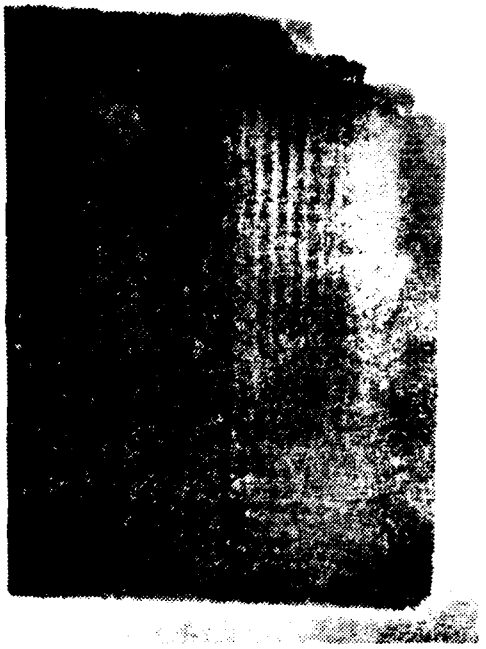


**Figure 2-5. Etch Pits in the CdTe Substrate of Array RH21-03 as a Result of Excessive Hybridization Force.** The etch pits are about 100 microns from the HgCdTe/CdTe interface. The pattern in the photograph is caused by modulation in the etch pit density which has a period of 102 microns, corresponding to the indium column spacing.

Computer modeling of the Ro data versus temperature suggests diffusion limited performance at 120 K and generation-recombination limited performance at 80 K.

The diffusion approximations used to fit data are as follows:

$$Ro(diff) = kT/qI_s \tag{2-1}$$

$$I_s = A_j q^2/kTn_i^2/N_A \mu_e L_e \tag{2-2}$$

where $A_j$ is the junction area, $n_i$ is the intrinsic carrier concentration, $N_A$ is the acceptor concentration, $L_e$ is the minority carrier electron diffusion length, and $\mu_e$ is the minority carrier electron mobility. Also for G-R approximations:

$$Ro\ (G\text{-}R) = kT/qI_o f(b),\ f(b) = 1 \tag{2-3}$$

and

$$I_o = n_i w_o A_j/\tau_o kT/V_{bi} \tag{2-4}$$

or

$$I_o = n_i s_o w_o PkT/V_{bi} \tag{2-5}$$

for depletion layer or surface g-r current respectively. For this case, $s_o$ is the surface recombination velocity inside the depletion region where it intersects the semiconductor surface, $w_o$ is the depletion width at zero bias voltage, P is the junction perimeter, $\tau_o$ is the effective depletion layer lifetime and $V_{bi}$ is the depletion built in voltage[10].

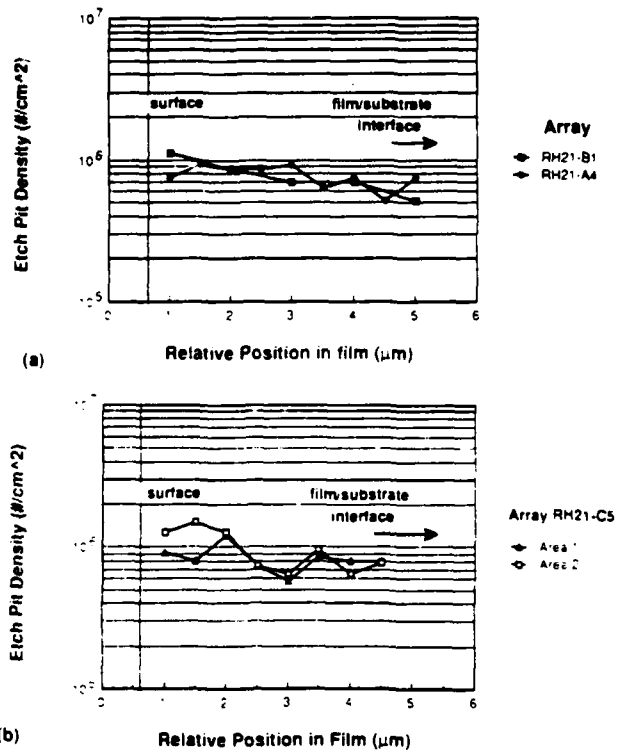



**Figure 2-6. Etch Pit Density Versus Depth for Three Arrays:** a) arrays RH21-A4 and RH21-B1 are unhybridized control samples and b) array RH21-C5 was hybridized with 3.9 x $10^7$ N/m$^2$, and sampled in two areas of the film

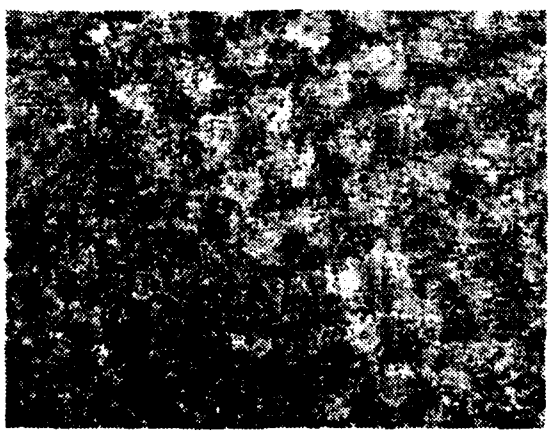


**Figure 2-7. Low Power Photomicrograph of Etch Density Modulation in Array RH21-C2 which was Hybridized with 5.9 x $10^7$ N/m$^2$.** Etch pit density at column locations was 9.6 x $10^6$/cm$^2$ and between the column locations was approximately 2.15 x $10^6$cm$^2$.

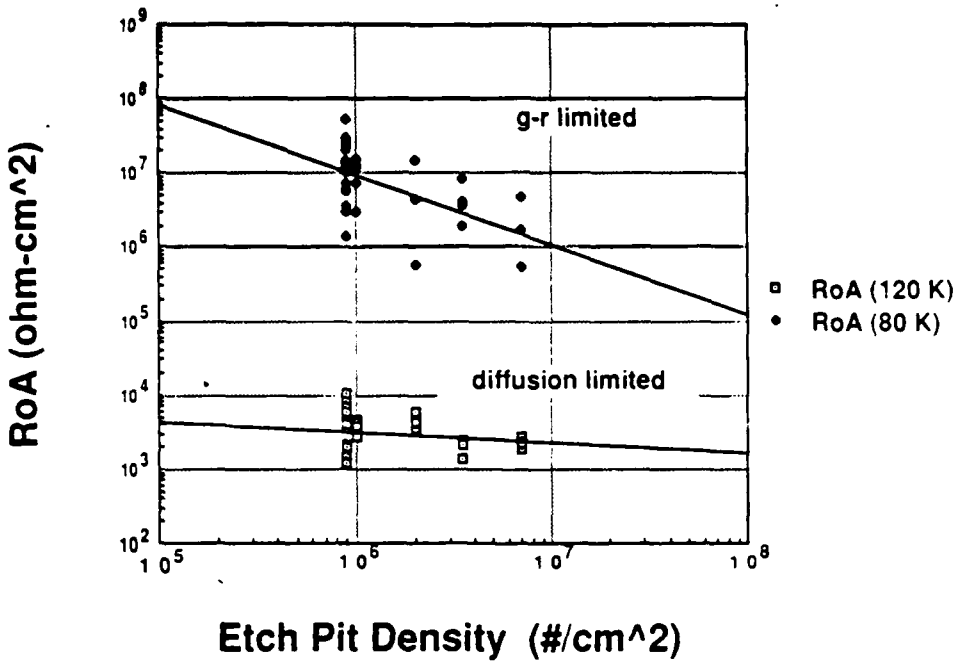



**Figure 2-8. Photodiode Zero Bias Impedance Multiplied by Junction Area ($R_oA$) Versus Etch Pit Density for 39 Elements from Four Arrays at 120 K and at 80 K.**

Figure 2-9 shows a typical computer modeled fit for data from one of the arrays for $R_oA$ versus 1000/T that suggests the array performance was diffusion limited at 120 K and g-r limited at 80 K. We were also able to fit the current voltage characteristics with a simple model involving diffusion and g-r mechanisms. We do not however have enough temperature dependent data to rule out the possibility of there being some tunneling current contributions.

Figure 2-10 shows modeled data for two individual diodes that correlate increased etch pit density with an increased g-r contribution at 120K from the larger surface recombination velocity ($s_o$) required to fit the 80 K data. Due to lack of any variable area data, surface g-r cannot be distinguished from bulk g-r contributions. The data shows that the dislocation density has a more pronounced effect on the dark current at the g-r limited temperature than at the diffusion limited temperature for the samples studied. Dislocations could act as Shockley-Read centers and it is therefore not surprising to see a strong dependence of the dark currents at the lower g-r limited temperature. At the diffusion limited temperature, the less pronounced effect of the dislocation density on the dark currents suggests that there was a source of diffusion current, possibly thermal or due to a high density of local defects or impurities which dominates over the contribution of the dislocations.

### 2.2.4 HFS Conclusions

The conclusions from this study are the following: dislocations were introduced into the HgCdTe epitaxial layers with hybridization forces greater than 4.8 x $10^7$ N/m$^2$. Dislocations were introduced into the CdTe substrates for hybridization forces of 9.4 x $10^7$ N/m$^2$. There were significantly increased dark currents observed in high etch pit density areas at a g-r limited operating temperature (80 K) and less pronounced increased dark currents observed in high EPD areas at a diffusion limited operating temperature (120 K). The data suggests that hybridization forces used in

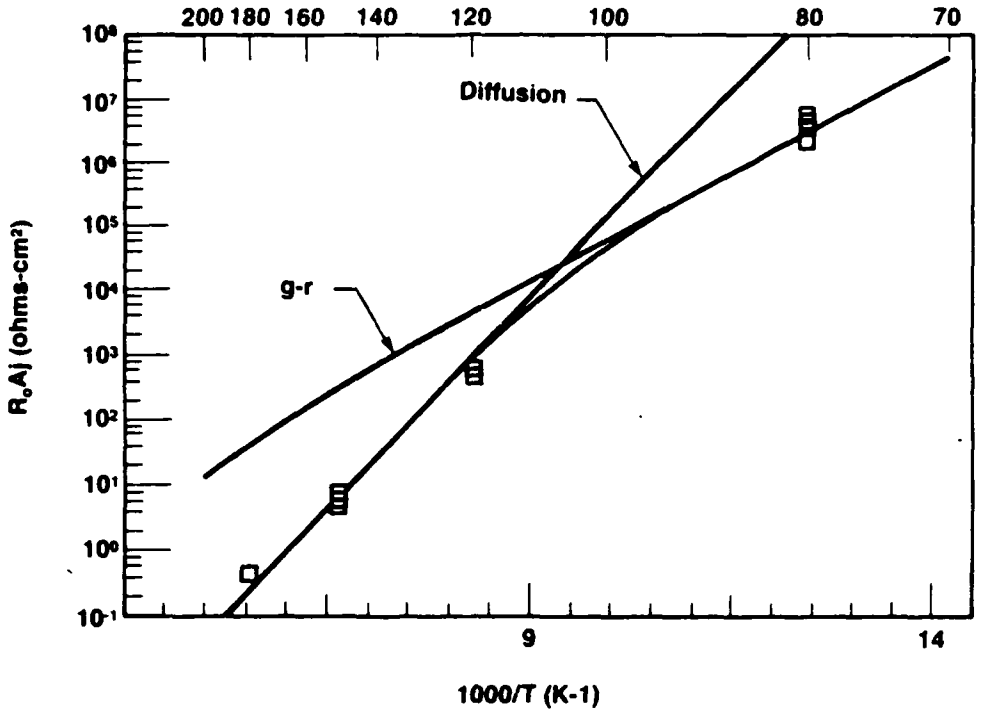



**Figure 2-9. Model of $R_oA$ versus 1000/T.** A simple model considering only diffusion and g-r currents suggests the devices are diffusion limited at 120 K and g-r limited at 80 K.

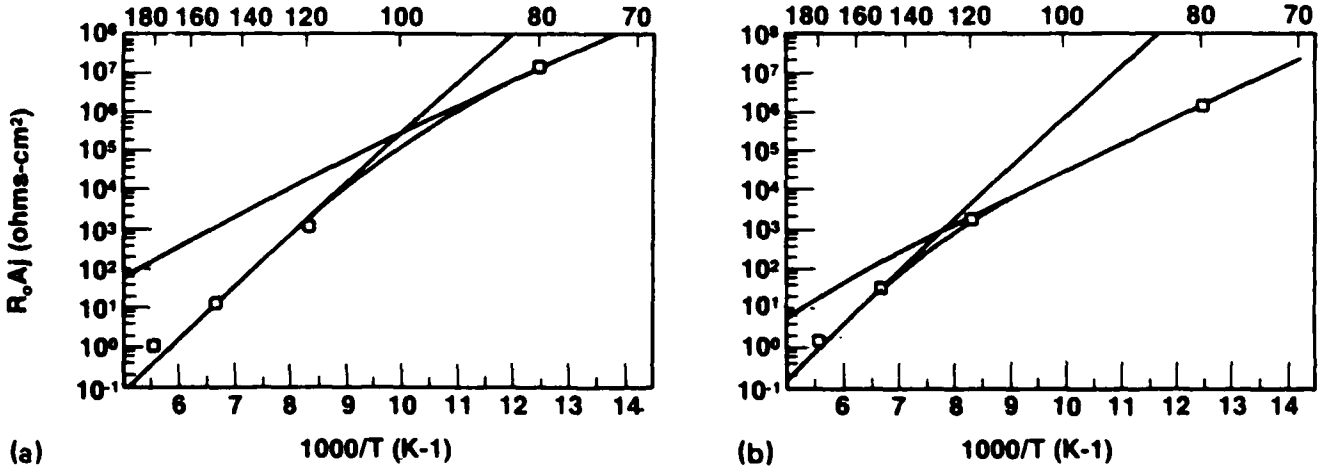



**Figure 2-10. Comparison of Modeled $R_oA$ Versus 1000/T for a Device in a) a Low EPD Area (1 x $10^6$/cm²) and in b) a High EPD (6 x $10^6$/cm²) Area.** Surface recombination velocity modeled to be a factor of two higher in the higher EPD area.

the fabrication of $Hg_{0.7}Cd_{0.3}Te$ should be kept below 4.8 x $10^7$ N/m$^2$ to avoid introducing potentially device degrading dislocations. The narrower bandgap and reduced microhardness[11] of $Hg_{0.8}Cd_{0.2}Te$ suggest that the longer wavelength focal plane arrays are more sensitive to hybridization force.

## 2.3 ENVIRONMENTAL STRESS TESTING

This portion of the program evaluated the effect of three environmental stresses on the performance of HgCdTe detector arrays. The stresses included evaluating the performance of arrays stored for approximately two years at room temperature in a dry nitrogen environment, vacuum baking of the arrays, and cycling the arrays from room temperature to operating temperature. The schematic in Figure 2-11 shows the process sequence for these studies.

### 2.3.1 Long Term Storage

The arrays used to evaluate the effect of long term storage on device performance were 32x32 element arrays with 4 mil pitch, fabricated on MW LPE HgCdTe in 1985 and 1986. The arrays were stored in dry nitrogen purged dry boxes during the approximately two years between initial test and the 1988 test for this program. The interconnect and $R_o$ data for these arrays are summarized in Table 2-3. The RH 13 and RH 21 arrays were passivated with ZnS and the RH 31 arrays were passivated with $SiO_2$.

The two ZnS passivated arrays showed improvement in Ro by 243% after the two year storage. These two arrays also received vacuum bakes and showed improvement in Ro after that treatment (data to follow). Modelling after the vacuum bake suggested that a reduction in g-r currents was the cause for the improvement in $R_o$, and it is inferred that the same mechanism is respon-

PURPOSE: Evaluate photovoltaic detector and focal plane array performance as a function of environmental stresses including vacuum baking and temperature cycling.

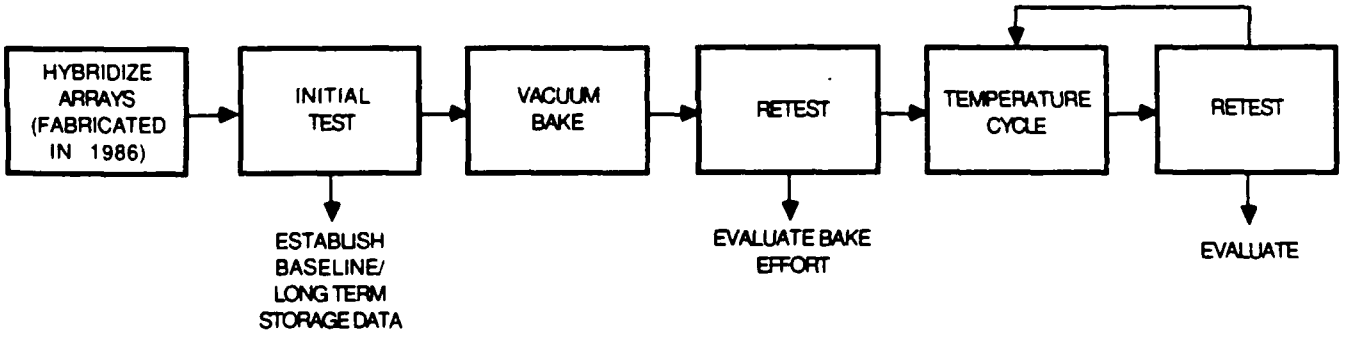



**Figure 2-11. Schematic Showing Environmental Stress Testing Plan**

**Table 2-3. Data Summary for Hybridized Arrays Stored in Nitrogen for Two Years**

| Device ID | 1986 DATA Ro(Ω) E+7 | 1986 DATA T=120K Interconnect | 1986 DATA Date | 1988 DATA Ro(Ω) E+7 | 1988 DATA T=120K Interconnect | 1988 DATA Date | Avg. Ro Variation % | Passivation |
|---|---|---|---|---|---|---|---|---|
| RH13D3 | 4.4 | 34 | 12/85 | 15.1 | 23 | 3/88 | 243 | ZnS |
| RH21C4 | 1.4 | 42 | 4/86 | 4.8 | 43 | 3/88 | 243 | ZnS |
| RH31D5 | 3.0 | 64 | 6/86 | 4.0 | 64 | 3/88 | 33 | $SiO_2$ |
| RH31C6 | 2.1 | 49 | 6/86 | 3.0 | 48 | 3/88 | 43 | $SiO_2$ |
| RH31D6 | 2.8 | 58 | 6/86 | 4.0 | 55 | 4/88 | 43 | $SiO_2$ |

sible for the improvement in $R_o$ after long term storage. The $SiO_2$ passivated arrays showed a far smaller performance change, also as an improvement. This is in contrast to the observed changes after vacuum bake, as will be discussed shortly.

### 2.3.2 Vacuum Bake

These tests were designed to simulate dewar bake out schedules which might be encountered when assembling detector/dewar units in a production environment. The arrays used in this portion of the study were in a 32x32 pixel configuration with 4 mil pitch and were fabricated in 1986 (two years prior to this work) using single layer MW LPE HgCdTe on CdTe. The arrays were passivated either with ZnS or $SiO_2$. The majority of the arrays used for the vacuum bake studies had also been hybridized and tested in 1986. Hence, the "initial test" data for vacuum bake was also a re-test after a two year storage. Following the initial test, the arrays were vacuum baked in a test dewar according to one of two bake schedules; 72 °C for 30 hours or 85 °C for 2 weeks. The arrays were again tested and the results analyzed.

Table 2-4 shows an overall summary of the six arrays which were vacuum baked. One array passivated with ZnS and one passivated with $SiO_2$ were baked at 72 °C for 30 hours. On both arrays, the average Ro increased, although more so for the ZnS passivated array. More interesting are the results on the four arrays baked at 85 °C for two weeks. Here a substantial difference in the post-bake test results is observed for the two passivation schemes. For the two ZnS passivated arrays, an improvement in the array average $R_o$ was seen. For the $SiO_2$ passivated arrays, however, the array average Ro decreased. This decrease, rather dramatic in the case of RH31-D6, prompted a deeper probe into the cause of the degradation. Detailed I-V measurements and modeling were done on several elements on the array.

The following expressions were used for modeling the IV characteristics for the detectors:

$$I(diff) = I_s\left(\exp(qV/kT)-1\right) \tag{2-6}$$

Where the terms are defined as usual, and

$$I(g\text{-}r) = I_o \frac{\exp(qV/2kT) - \exp(-qV/2kT)}{1-\sqrt{1-V/V_{bi}}} \cdot f(b) \tag{2-7}$$

Where:

$$I_o = \frac{n_i w_o A_j}{\tau_o} \frac{kT}{V_{bi}} \tag{2-8}$$

## Table 2-4. Overall Summary of Vacuum Bake Data

| | BEFORE BAKE | | | AFTER BAKE | | | PASSIVATION |
|---|---|---|---|---|---|---|---|
| Array | | | RH21C4 | | | | |
| DATE | | Before Bake | | | 30 hrs @72°C | | |
| TEMP (K) | 120 | 150 | 180 | 120 | 150 | 180 | |
| Ro (Ω) | 4.76E+7 | 6.24E+5 | 2.65E+4 | 5.65E+7 | 6.74E+5 | 3.02E+4 | |
| Rs (Ω) | 9.26E+4 | 4.58E+4 | 1.94E+4 | 2.30E+5 | 1.25E+5 | 5.77E+2 | ZnS |
| Q.E. (%) | 88 | 69 | 72 | 96 | 97 | 40 | |
| Noise (A) | 6.32E-13 | 3.37E-12 | 1.46E-11 | 6.76E-13 | 2.54E-12 | 1.36E-11 | |
| Interconnect | 13op/2sh/2p | 11op/2sh/5p | 11op/2sh/10p | 15op/1p | 17op | 17op | |
| Array | | | RH31D5 | | | | |
| DATE | | Before Bake | | | 30 hrs @72°C | | |
| TEMP (K) | 120 | 150 | 180 | 120 | 150 | 180 | |
| Ro (Ω) | 3.06E+7 | 7.43E+5 | 5.27E+4 | 3.19E+7 | 6.61E+5 | 4.57E+4 | |
| Rs (Ω) | 5.08E+3 | 4.47E+3 | 2.48E+3 | 2.82E+3 | 2.95E+3 | 1.95E+3 | |
| Q.E. (%) | 35 | 21 | 10 | 57 | 41 | 12 | $SiO_2$ |
| Noise (A) | 5.33E-13 | 2.69E-12 | 1.15E-11 | 7.30E-12 | 3.37E-12 | 1.20E-11 | |
| Interconnect | 1c,en | 1open | 1open | 1open/2p | 1open/1sht | 1open | |
| Array | | | RH31C6 | | | | |
| DATE | | 3/23/88 | | | 2 wks @85°C | | |
| TEMP (K) | 120 | 150 | 180 | 120 | 150 | 180 | |
| Ro (Ω) | 2.98E+07 | 5.94E+05 | 4.18E+04 | 2.27E+07 | 5.20E+05 | 3.86E+04 | |
| Rs (Ω) | 3.42E+03 | 3.40E+03 | 2.27E+03 | 4.47E+03 | 4.25E+03 | 2.90E+03 | $SiO_2$ |
| Q.E. (%) | 58 | 38 | 19 | 66 | 28 | 6 | |
| Noise (A) | 5.53E-13 | 3 106E-12 | 1.33E-11 | 6.53E-13 | 3.42E-12 | 1.74E-11 | |
| Interconnect | 16open | 16open | 16open | 26open/2p | 25open/1p | 25open | |
| Array | | | RH31D6 | | | | |
| DATE | | Before Bake | | | 2 wks @85°C | | |
| TEMP (K) | 120 | 150 | 180 | 120 | 150 | 180 | |
| Ro (Ω) | 3.98E+07 | 6.38E+05 | 4.10E+04 | 9.19E+05 | 8.84E+05 | 2.62E+04 | |
| Rs (Ω) | 4.98E+03 | 3.24E+03 | 1.74E+03 | 1.88E+04 | 1.78E+04 | 1.49E+04 | |
| Q.E. (%) | 53 | 25 | 7 | 33 | 34 | 18 | $SiO_2$ |
| Noise (A) | 5.00E-13 | 4.85E-11 | 1.33E-11 | 4.29E-11 | 2.70E-12 | 5.98E-11 | |
| Interconnect | 4sht/4L/1op | 4sht/4L/1op | 4sht/3L/1op | 12open/4sht | 12open/4sht | 12open/4sht | |
| Array | | | RH11C2 | | | | |
| DATE | | Before Bake | | | 2 wks @ 85°C | | |
| TEMP (K) | 120 | 150 | 180 | 120 | 150 | 180 | |
| Ro (Ω) | 1.46E+07 | 3.04E+05 | 1.83E+04 | 3.16E+07 | 4.93E+05 | 2.30E+04 | |
| Rs (Ω) | 1.46E+03 | 9.34E+02 | 7.58E+02 | 4.36E+03 | 3.75E+03 | 2.20E+03 | |
| Q.E. (%) | 76 | 42 | 46 | 81 | 105 | 47 | ZnS |
| Noise (A) | 1.46E-12 | 5.00E-12 | 5.91E-11 | 1.22E-12 | 4.00E-12 | 8.14E-11 | |
| Interconnect | 6open/12p | 6open/17P | 5op/43P | 9open/1sht | 7op/1P/1S/1R | 9op/1sht | |
| Array | | | RH13D3 | | | | |
| DATE | | Before Bake | | | 2 wks @ 85°C | | |
| TEMP (K) | 120 | 150 | 180 | 120 | 150 | 180 | |
| Ro (Ω) | 1.51E+08 | 2.12E+06 | 8.96E+04 | 5.09E+08 | 4.72E+06 | 1.19E+05 | |
| Rs (Ω) | 1.73E+03 | 1.47E+03 | 1.34E+03 | 5.54E+03 | 3.48E+03 | 2.73E+03 | ZnS |
| Q.E. (%) | 60 | 17 | 28 | 60 | 32 | 7 | |
| Noise (A) | 4.45E-13 | 1.63E-12 | 8.66E-12 | 3.82E-13 | 1.18E-12 | 1.41E-11 | |
| Interconnect | 28sht/12R/1op | 1op/27sht/4R | 27sht/1op | 29sht/2op/1P | 29sht/2op | 29sht/2op | |

For depletion layer g-r and:

$$I_o = n_i s_o w_o P \frac{kT}{V_{bi}} \quad (2\text{-}9)$$

for surface g-r. The term f(b), which is an analytic function describing the effects of trapping, was set equal to 1, for the case of most effective g-r centers.[12] No tunneling was assumed. Figure 2-12 shows the results of this modeling for RH31-D6, element #31. The IV (at T=120 K) prior to the bake showed a reverse characteristic which was chiefly diffusion current limited. The model indicated that the g-r current was only of the order $5.4 \times 10^{-11}$ amp. After the bake, the reverse current increased significantly. The model now indicated that the g-r current at zero bias had increased to $2.5 \times 10^{-8}$ amp, a factor of 463 increase. The fact that the degradation of $SiO_2$ - passivated devices was due to an increase in the g-r current points to a degradation of the surface passivation, which was not observed for the ZnS passivated arrays.

Table 2-5 presents a summary of detailed I-V measurements which were done. It can be seen that for the ZnS and $SiO_2$ passivated arrays baked at 72 °C for 30 hours there is little change in the measured and modeled parameters. Both of the arrays modeled after the 85 °C, 2 week bake showed degradation, chiefly in the g-r current. Since no degradation in the Ro of the ZnS passivated arrays was observed, no detailed I-V modeling was done. The cause for the increase of the Ro on the ZnS passivated arrays might be due to a reduction in the g-r current, due to favorable shifting of charge in the passivation layer. These data suggest that ZnS is preferred over $SiO_2$ for arrays which must be baked at 85 °C for 2 weeks.

### 2.3.3 Temperature Cycling

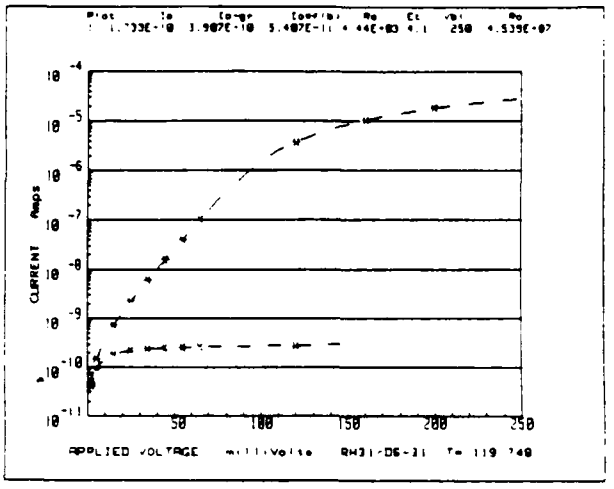
Temperature cycling between room temperature and 80 K was done on MW and LW arrays in different configurations. The arrays included two MW 32x32 mosaic arrays with 4 mil pitch, which were hybridized to leadout boards. Two LW test arrays, which were delivered to NRL, were also included in the sample. Finally, one 240x2 MW scanning array, approximately 380 mil long, was hybridized to a Si Mux. The 32x32 element array results are summarized in Table 2-6. Prior to temperature cycling, these arrays received a 72 °C, 32 hour bake, the results of which were discussed earlier. Although temperature cycling was done from room temperature to 80 K, these arrays were tested for variations in Ro, series resistance Rs, quantum efficiency, noise and interconnect at 120 K, due to test station limitations. Additional data were taken at 150 and 180 K. In the case of array RH31-D5, the data were taken after 4, 14 and 24 cycles. Although some variations in array average Ro were observed at each test, they were not significant, and were more pronounced at 120 K. At 120 K, the devices have a larger g-r current component than at the higher temperatures. The observed variations are likely due to changes in surface leakage, although detailed modeling was not done. No major changes in quantum efficiency were seen between the 14 and 24 cycle.

Data for RH 21-C4 are also shown in Table 2-6. It can be readily seen that the detector performance varied in a non-monotonic fashion at each test point. This array also showed an increasing number of opens with temperature cycling, a trend which began in the vacuum bake studies. The conclusion is that this array was poorly hybridized initially, and that gave rise to additional interconnect loss with temperature cycling. The poor hybridization could be due to bump contamination and/or poor parallelism adjustment during hybridization. It is not appropriate to draw conclusions about the effect of temperature cycling on ZnS passivated MW devices from these data, since data on LW devices which are more sensitive to passivation effects do not show similar degradation (data to follow).

$I_{sat}$(diffusion) = 1.733 x $10^{-10}$ amps

$I_{ogr}$f(b) = 5.41 x $10^{-11}$ amps

$R_o$ = 4.5 x $10^7$ ohms

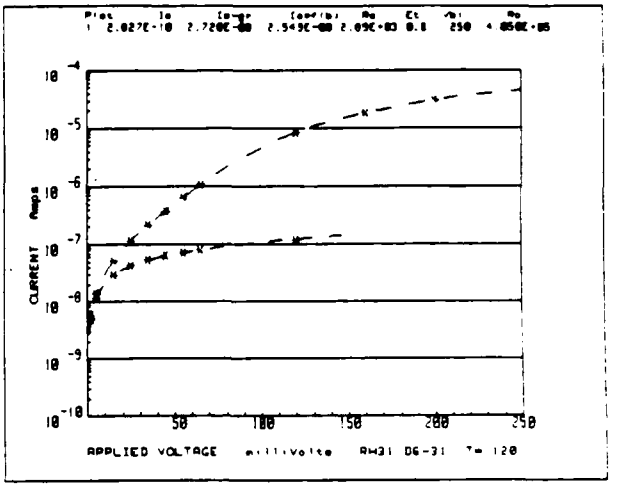



before bake

$I_{sat}$(diffusion) = 2.827x $10^{-10}$ amps

$I_{ogr}$f(b) = 2.543 x $10^{-8}$ amps

$R_o$ = 4.1 x $10^5$ ohms




after bake

**Figure 2-12. Detailed I-V Analysis of element #31 of the $SiO_2$ Passivated Array RH31-D6 After a 2-Week 85 °C Bake Shows a Significant Increase in g-r Current (Surface Passivation Degeneration)**

**Table 2-5. $SiO_2$ Passivated Arrays Show Significant Increases in g-r Current After 85 °C Vacuum Bake. ZnS Passivated Arrays are Stable to 85 °C Bake**

| Array | Element | Ro ($10^7$) | Ro After Bake ($10^7$) | (120 K DATA) Before $I_{sat}$ ($10^{-10}$ A) | Before $I_{g-r}$ ($10^{-11}$ A) | After $I_{sat}$ ($10^{-10}$ A) | After $I_{g-r}$ ($10^{-11}$) | Passivation |
|---|---|---|---|---|---|---|---|---|
| RH21-C4 (72° C, 30 hrs) | "all" | 5.2 | 5.7 | | | | | ZnS |
| | 29 | 6.9 | 6.2 | 1.2 | 5.3 | 1.4 | 4.2 | |
| | 57 | 6.8 | 6.4 | 1.2 | 3.0 | 1.3 | 3.4 | |
| RH31-D5 (72° C, 30 hrs) | "all" | 3.1 | 3.9 | | | | | $SiO_2$ |
| | 41 | 3.4 | 3.4 | 2.1 | 9.1 | 2.4 | 6.9 | |
| | 55 | 3.1 | 2.9 | 2.3 | 9.8 | 2.7 | 8.1 | |
| | 29 | 3.4 | 3.2 | 2.3 | 7.4 | 2.5 | 7.7 | |
| RH31-C6 (85° C, 2 weeks) | "all" | 3.0 | 2.3 | | | | | $SiO_2$ |
| | 41 | 3.4 | 3.1 | 2.4 | 6.6 | 1.7 | 17.1 | |
| RH31-D6 (85° C, 2 weeks) | "all" | 4.0 | 0.092 | | | | | $SiO_2$ |
| | 31 | 4.5 | 0.041 | 1.7 | 5.4 | 2.8 | 2543.0 | |

## Table 2-6. Summary of Temperature Cycling Data on Arrays RH31-D5($SiO_2$)and RH21-C4 (ZnS)

| Array | | | RH31D5 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| DATE | | 3/24/88 | | | 5/23/88 | | | 6/20/88 | |
| TEMP (K) | 120 | 150 | 180 | 120 | 150 | 180 | 120 | 150 | 180 |
| Ro (Ω) | 3.19E+7 | 6.61E+5 | 4.58E+4 | 3.59E+7 | 7.16E+5 | 4.72E+4 | 4.43E+7 | 7.61E+5 | 5.17E+4 |
| Rs (Ω) | 2.82E+3 | 2.95E+3 | 1.95E+3 | 2.41E+3 | 2.59E+3 | 2.05E+3 | 2.36E+3 | 2.59E+3 | 1.74E+3 |
| Q.E. (%) | 57 | 41 | 12 | 64 | 63 | 20 | 64 | 65 | 23 |
| Noise (A) | 7.30E-12 | 3.37E-12 | 1.20E-11 | 1.37E-11 | 3.00E-12 | 1.30E-11 | 1.10E-12 | 3.00E-12 | 9.10E-11 |
| Interconnect | 1open/2P | 1open | 1open | 1open | 1open | 1open | 2open | 1open | 1open |
| # Cycles | | 4 | | | 14 | | | 24 | |
| Array | | | RH21C4 | | | | | | |
| DATE | | 3/24/88 | | | 5/25/88 | | | 6/21/88 | |
| TEMP (K) | 120 | 150 | 180 | 120 | 150 | 180 | 120 | 150 | 180 |
| Ro (Ω) | 5.65E+7 | 6.74E+5 | 3.02E+4 | 3.62E+7 | 8.44E+5 | 7.20E+4 | 6.74E+7 | 7.28E+5 | 2.90E+4 |
| Rs (Ω) | 2.30E+5 | 1.25E+5 | 5.77E+2 | 1.23E+6 | 2.47E+5 | 7.14E+4 | NA | 8.24E+2 | NA |
| Q.E. (%) | 96 | 97 | 40 | 104 | 85 | 75 | 109 | 90 | 36 |
| Noise (A) | 6.76E-13 | 2.22E-12 | 1.36E-11 | 8.68E-13 | 2.69E-12 | 1.79E-11 | 7.67E-13 | 2.45E-12 | 1.46E-11 |
| Interconnect | 15open/1P | 17open | 17open | 24open | 25open | 24open | 29open | 29open | 28open |
| # Cycles | | 5 | | | 15 | | | 25 | |

- **Arrays were cycled down to 80 K and then brought to 120 K for testing.**

The temperature cycling data for two LW test arrays are shown in Figure 2-13. These arrays were temperature cycled 21 times from room temperature to 80 K, and diode performance was tested at 80 K. Virtually no change in the array average of detector impedance or responsivity were observed.

The MW 240x80 element array was used to provide the most severe test of interconnect stability in this evaluation. The array is approximately 380 mil long, and was hybridized to a Si MUX. Hence, the assembly had the maximum anticipated thermal expansion coefficient mismatch. The interconnect data for this array, taken through the mux, are shown in Figure 2-14 as a function of temperature cycling. The interconnect did not change appreciably between the initial data and the fifth temperature cycle (the vertical bars on the initial data are mux artifacts). Between the fifth and twentieth cycle, however, significant interconnect loss occurred at one end of the array.

Failure analysis on this assembly was done. Figure 2-15 shows examples of indium columns which illustrate both good and poor cold welding. These examples are portions of detector arrays which were removed from their mating circuit boards. The left hand micrograph shows evidence of excellent cold welding. This is seen by the indium plastic deformation and "draw" which occurred during array removal. This type of behavior consistently results in stable, reliable interconnect. An example of poor cold welding is shown in the right hand micrograph. Notice that there is no indication of welding between the column on the circuit board (shown) and its mating array column. This can be caused by contamination or oxides present on the column prior to hybridization, force vs. time schedule during hybridization, and column geometries. It was suspected that this failure mechanism was responsible for the observed interconnect loss on the 240x8 array.

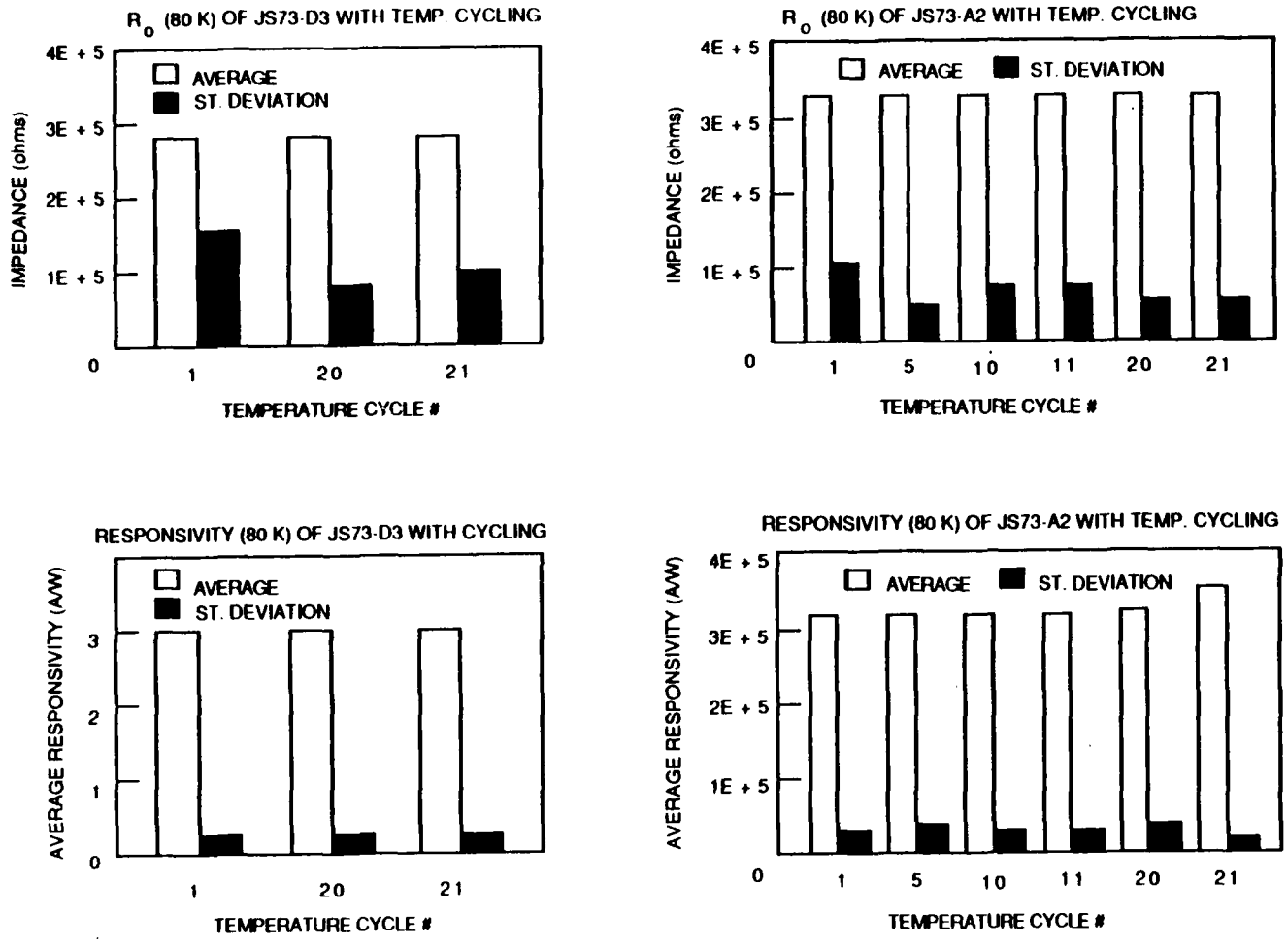
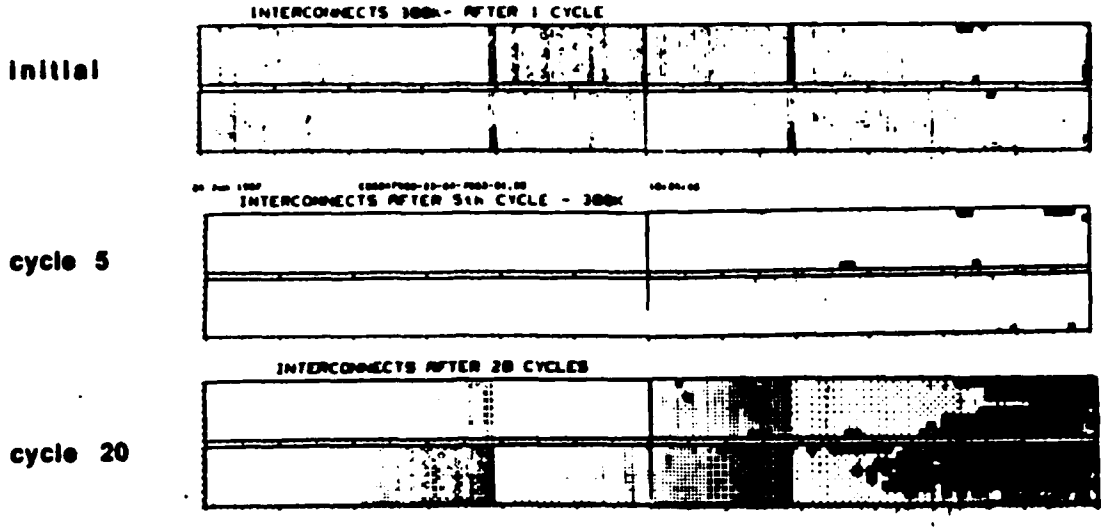



**Figure 2-13. Temperature Cycling Data for LW Test Arrays (0.180" x 0.75") Delivered on the Program Show No Degradation in Performance or Interconnects After 21 Temperature Cycles**




- black indicates an "open"
- Interconnect failures are being analyzed for mechanism

**Figure 2-14. Interconnect Map of 240 x 8 Array with Temperature Cycling Show Loss of Interconnect at One End of the Array**

Removal of the 240x8 array from the multiplexer showed otherwise. Instead of finding smooth separation between the array and multiplexer columns, the observations indicated that the separation occurred between the indium column and the HgCdTe surface (Figure 2-16). The poor adhesion between the contact metal (on which the indium was deposited) and the HgCdTe surface was likely due to surface contamination, and is not directly related to hybridization technology. This shows, however, that many factors can affect good interconnect yield.

### 2.3.4 Environmental Stress Testing Summary

The environmental stress testing task evaluated the effects of long term storage, vacuum bake and temperature cycling (RT to 80 K) on MW and LW HgCdTe detector arrays, both in terms of detector performance and interconnect yield. The electrical properties (measured in terms of average array Ro) of both the ZnS and $SiO_2$ passivated arrays improved with two year storage at room temperature, far more in the case of the ZnS passivated arrays than for $SiO_2$. This is likely due to a reduction in the g-r component of the noise current, which can be related to surface passivation. One possible mechanism is shifting of charge in the insulator over time, with a favorable effect on the surface potential. Vacuum baking, at schedules equivalent to those used in dewar bakeout prior vacuum sealing, produced a significant increase in g-r currents on $SiO_2$ passivated arrays. This was not observed on arrays passivated with ZnS, whose performance actually improved with baking. Hence, from these data, the ZnS would prove to be the passivation of choice over $SiO_2$.

Temperature cycling studies showed that no significant effect on device performance is introduced as a result of such cycling. Arrays which had good interconnect to begin with seemed to maintain the level of interconnect. This was true, except in the case of the 240x8 FPA, which had interconnect failure at one end as observed after a total of 20 cycles. Failure analysis showed that

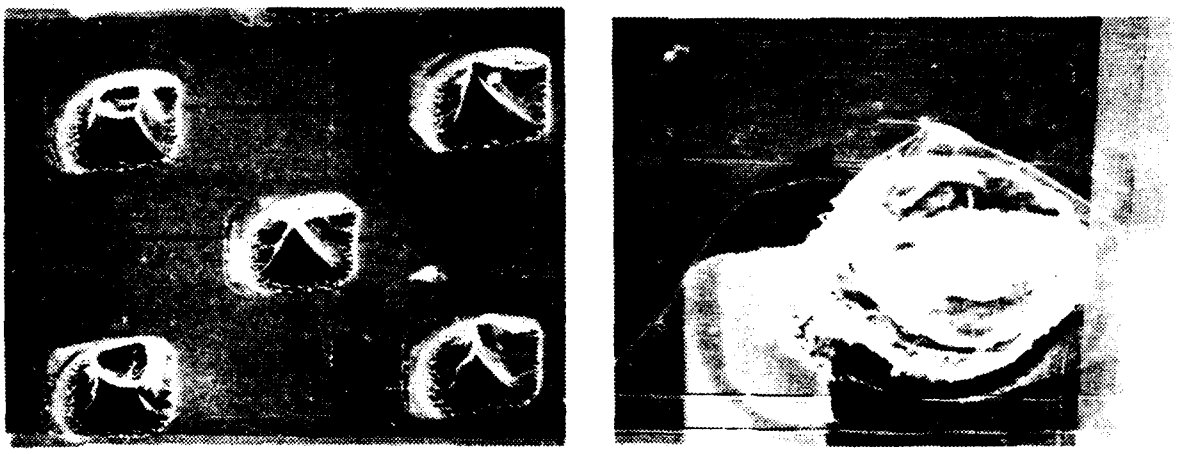


**Figure 2-15. Examples of Qualitative Data from a Forced Separation of a Focal Plane Showing Poor and Good Interconnect Quality**

this failure was due to poor adhesion between the contact metal (onto which that indium column had been deposited) and the HgCdTe. This prevents a firm conclusion about long term interconnect reliability of large ( ~ 380 mil long) focal planes to be reached.

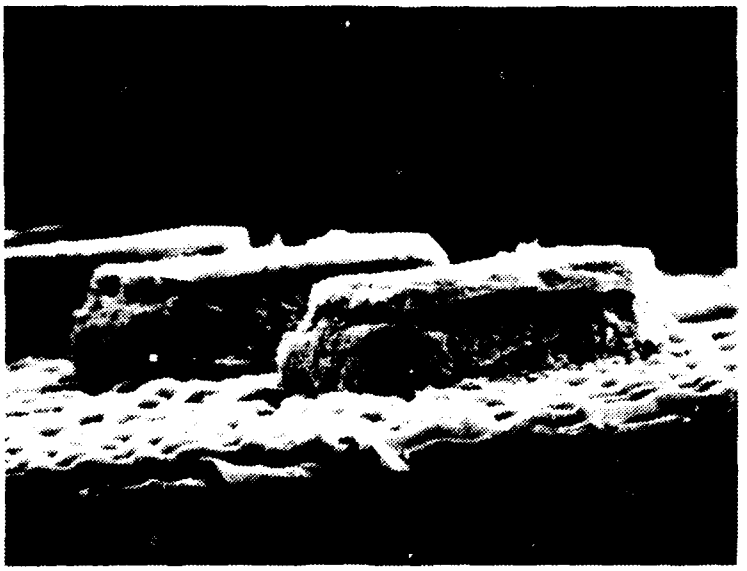


**Figure 2-16. Failure Analysis of Interconnect Loss on a 240x80 Format FPA Shows Failure at the Indium Column/HgCdTe Interface**

# SECTION 3
# CONCLUSIONS

The conclusions are summarized as follows:

1) Dislocations can be introduced into the detector material during hybridization. These were observed to have greater density as the hybridization forces were increased.

2) The dislocations can cause significantly increased dark currents in g-r limited MW devices.

3) ZnS passivated boron-implanted detector arrays were stable after 2 weeks of vacuum baking at 85 °C, followed by 20 temperature cycles.

4) $SiO_2$ passivated boron-implanted detector arrays show no degradation after a 30 hours vacuum bake at 72 °C, but showed degradation after a 2 week vacuum bake at 85 °C.

5) Indium cold welding using high aspect ratio indium columns has led to improved interconnect reliability.

# SECTION 4
# ACKNOWLEDGEMENTS

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# SECTION 5
# REFERENCES


1. J.G. Fleming, et. al., *Proc. 3rd Int. Conf. on II-VI Compounds,* Monterey, CA (1987)
2. M.R. Kruer, D.A. Scribner, and J.M. Killiany, Optical Engineering **26,** 182, (1987)
3. Yoshihiro Miyamoto, Hiroshi Sakai and Kunihiro Tanikawa, Proc. of SPIE **572,** 115 (1985)
4. J.H. Tregilgas, T.L. Polgreen and M.C. Chen, J. of Crystal Growth **86,**460 (1988).
5. J.A. Mrozckowski and H.R. Vydyanath, J. Electrochem. Soc. **128,** 655, (1981).
6. K. Nakagawa, K. Maeda, and S. Takeuchi, Appl. Phys. Lett. **34,** 574, (1979).
7. E.L. Polisar, N.M. Boinykh, G.V. Indenbaum, A.V. Vanyukov, and V.P. Schastlivyi, J. Sov. Phys **11,** 48, (1968).
8. M. Grimbergen and A. Szilagyi, Mat. Res. Soc. Symp. Proc. **69,** 257, (1986)
9. *Private communications with Andrei Szilagy.*
10. R.J. Briggs, J.W. Marciniec, P.H. Zimmermann and A.K. Sood, IEDM, (1980).
11. M. Schenk and A. Fissel, J. Crystal Growth **86,** 502, (1988)
12. C.T. Sah, R.N. Noyce and W. Shockley, Proc. IRE 45, 1228 (1957).